Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched and stored;

a fetch address operation circuit that calculates a fetch address, the fetch address being used to fetch and store an instruction code in the instruction queue;

a fetch circuit that fetches an instruction code, the instruction code being read out from a memory based on the fetch address and being stored into the instruction queue; and

a branch information setting circuit that decodes a branch setting instruction, the branch setting instruction explicitly or implicitly specifying a branch occurring address and a branch target address, a branch to the branch target address occurring when the fetch address is the branch occurring address after a x-th instruction from the branch setting instruction, x being a non-zero positive integer, the branch information setting circuit storing the branch occurring address in a branch occurring address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded,

the fetch address operation circuit including a circuit that compares one of a previous fetch address and an expected next fetch address with a value stored in the branch occurring address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

2. (Currently Amended): A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched and stored;

a fetch address operation circuit that calculates a fetch address, the fetch address being used to fetch and store an instruction code in the instruction queue;

a fetch circuit that fetches an instruction code, the instruction code being read out from a memory based on the fetch address and being stored into the instruction queue; and

a branch information setting circuit that decodes a branch setting instruction, the branch setting instruction explicitly or implicitly specifying a branch occurring address and a branch target address, a branch to the branch target address occurring when the fetch address is the branch occurring address after a x-th instruction from the branch setting instruction, x being a non-zero positive integer, the branch information setting circuit storing the branch occurring address in a branch occurring address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded,

the fetch address operation circuit including a circuit that compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch occurring address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch occurring address storage register, or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch occurring address storage register.

3. (Previously Presented): The data processing device as defined in claim 1:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction; and

the fetch address operation circuit including a circuit that outputs a value that is stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address occurs reaches the loop count.

4. (Previously Presented): The data processing device as defined in claim 2:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction; and

the fetch address operation circuit including a circuit that outputs a value that is stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address occurs reaches the loop count.

5. (Previously Presented): The data processing device as defined in claim 1:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit including a circuit that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

6. (Previously Presented): The data processing device as defined in claim 2:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit including a circuit that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

7. (Previously Presented): The data processing device as defined in claim 3:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit including a circuit that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

8. (Previously Presented): The data processing device as defined in claim 4:

the branch setting instruction including a loop instruction that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit decoding the loop instruction, and storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit including a circuit that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

9. (Previously Presented): The data processing device as defined in claim 3:

the loop instruction having no branch target address information in an operand; and

the branch information setting circuit including a circuit that calculates the branch target address based on the address in memory where the loop instruction is stored and a fixed value and stores the calculated value in the branch target address storage register.

10. (Previously Presented): The data processing device as defined in claim 4:

the loop instruction having no branch target address information in an operand; and

the branch information setting circuit including a circuit that calculates the branch target address based on the address in memory where the loop instruction is stored and a fixed value and stores the calculated value in the branch target address storage register.

11. (Previously Presented): The data processing device as defined in claim 5:

the loop instruction having no branch target address information in an operand; and

the branch information setting circuit including a circuit that calculates the branch target address based on the address in memory where the loop instruction is stored and a fixed value and stores the calculated value in the branch target address storage register.

12. (Previously Presented): The data processing device as defined in claim 6:

the loop instruction having no branch target address information in an operand; and

the branch information setting circuit including a circuit that calculates the branch target address based on the address in memory where the loop instruction is stored and a fixed value and stores the calculated value in the branch target address storage register.

13. (Previously Presented): Electronic equipment comprising:

the data processing device as defined in claim 1;

means for receiving input data; and

means for outputting a result of a process performed by the data processing device based on the input data.

14. (Previously Presented): Electronic equipment comprising:

the data processing device as defined in claim 2;

means for receiving input data; and

means for outputting a result of a process performed by the data processing device based on the input data.

15. (Previously Presented): Electronic equipment comprising:
the data processing device as defined in claim 3;
means for receiving input data; and
means for outputting a result of a process performed by the data processing device based on the input data.

16. (Previously Presented): Electronic equipment comprising:
the data processing device as defined in claim 4;
means for receiving input data; and
means for outputting a result of a process performed by the data processing device based on the input data.

17. (Previously Presented): Electronic equipment comprising:
the data processing device as defined in claim 5;
means for receiving input data; and
means for outputting a result of a process performed by the data processing device based on the input data.

18. (Previously Presented): Electronic equipment comprising:
the data processing device as defined in claim 6;
means for receiving input data; and
means for outputting a result of a process performed by the data processing device based on the input data.